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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: ROCHE ET AL.	
Serial No. 10/039,765	Examiner: N.PATEL
Confirmation No. 9186	Art Unit: 2112
Filing Date: NOVEMBER 7, 2001	Attorney Docket No. 00RO3045288
For: SYNCHRONOUS DATA TRANSMISSION METHOD	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the final Office Action of November 1, 2007, and in connection with the Notice of Appeal filed concurrently herewith, please consider the remarks set out below.

REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application. Claims 20-46 and 48-52 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Claimed Invention

The present invention, as recited in independent Claim 20, for example, is directed to a method of transmitting data between two devices via a clock line and at least one data line,

with the clock line being maintained by default on a first logic value. The method comprises providing each device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value. The clock line is tied to the second logic value, via the two devices, after data is applied to the data line. The tie to the clock line is maintained by the device to which the data is sent while the device has not read the data. The method further comprises maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent.

Independent Claims 32, 44, 46, 48 and 51 are similar to independent Claim 20.

II. The Claims Are Patentable

The Examiner rejected independent Claims 20, 32 and 48 over the SPI Block Guide in view of the System Management Bus (SMBus) Specification. The Examiner also rejected independent Claims 44 and 46 over the SPI Block Guide, and independent Claim 51 over the SMBus Specification. All of the claim rejections will be discussed below.

The present invention provides a double control of the line by which each device - a master or a slave - can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly in the event of disparity of clock frequencies or when one of the devices

operates in multitasking on applications that have priority over the data transmission itself.

The Applicants submit that since the clock line in the SPI Block Guide is under the control of a master device, then there is simply no motivation to modify the SPI Block Guide in view of the SMBus Specification. Reference is directed to FIG. 4-1 on page 26 in the SPI Block Guide, for example, where there is no pull-up or pull-down of the clock SCK line. The clock is entirely under the control of the master device which uses a Baud Rate Generator to emit the clock signal.

Also in the SPI Block Guide, there is no tying of the clock signal from a default value to a second value. The slave, too, simply has a shift register to count the clock pulses, and thereby to synchronize itself to the clock signal. This is also confirmed on page 23, section 4.1, lines 11-12 in the SPI Block Guide, which provides: "When a data transfer operation is performed, this 16-bits register is serially shifted eight positions by the S-clock from the master, so data is exchanged between the master and the slave." (Emphasis added).

However, the Examiner has taken the position that FIG. 4-2 on page 27 in the SPI Block Guide illustrates that the clock line is maintained by default on a first logic value (SCK=1), and that one of the devices has the ability to tie the clock line to a potential representing a second logic value opposite the first logic value (SCK=0 at SCK Edge No. 1). The Applicants submit this figure is not relevant. In FIG. 4-2, the clock line SCK alternates between the high and the low state (when CPOL=1), but

does not teach or suggest how the clock signal SCK is controlled by the devices exchanging data.

Referring now to the SMBus Specification, it fails to teach or suggest tying the clock line to the second logic value, via the two devices, after data is applied to the data line, as in the claimed invention. Referring to page 9, lines 2-3, which provides: "Generally, a bus master device initiates a bus transfer between it and a single bus slave and provides the clock signals." (Emphasis added). Reference is also directed to page 20, section 4.3.1 titled Synchronization, lines 5-6, which provides: "A high-to-low transition on the SMBCLK line will cause all devices involved to start counting off their LOW period and start driving SMBCLK low if the device is a master".

The SMBus Specification thus fails to teach or suggest that both the master and the slave device can tie the clock line to a second logic value opposite the first logic value. Instead, only the master device can tie the clock line to a different potential.

The Applicants submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not provided. Accordingly, it is submitted that independent Claim 20 is patentable over the SPI Block Guide in view of the SMBus Specification. Independent Claims 32 and 48 are similar to independent Claim 20. It is submitted that independent Claims 32 and 48 are also patentable over the SPI Block Guide in view of the SMBus Specification.

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Independent Claims 44, 46 and 51 are similar to independent Claim 20. It is submitted that independent Claims 44 and 46 are patentable over the SPI Block Guide, and independent Claim 51 is patentable over the SMBus Specification. In view of the patentability of independent Claims 20, 32, 44, 46, 48 and 51, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 2 day of January, 2008.